AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of configuring a programmable logic device (PLD) comprising a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells, the method comprising:

initiating a configuration sequence for the PLD;

initiating a built in self test (BIST) procedure on the first array;

setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array;

wherein a respective error flag is associated with each column of RAM cells in the first array;

loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells; and

wherein the loading comprises generating for each column of RAM cells a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells, and selecting for input to [[the]] each column of RAM cells in response to the respective selection signal, one of a first set of bits of configuration data addressed to the column of RAM cells and a second set of bits of configuration data addressed to the adjacent column.

2. (Currently Amended) The method of Claim 1, wherein the PLD comprises a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells, the method further comprising:

initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array;

setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array; and

wherein a respective error flag is associated with each column of RAM cells in the second array;

loading second PLD configuration data for the PLD into the second RAM circuit, wherein when the second error flag is set the second PLD configuration data bypasses the second defective column of the RAM cells and a second portion of the second PLD configuration data is loaded into the second redundant column of the RAM cells; and

wherein the loading comprises generating for each column of RAM cells in the second array a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells in the second array, and selecting for input to [[the]] each column of RAM cells in response to the respective selection signal, one of a first set of bits of configuration data addressed to the column of RAM cells in the second array and a second set of bits of configuration data addressed to the adjacent column in the second array.

3. (Original) The method of Claim 1, wherein initiating a configuration sequence for the PLD comprising powering up the PLD.

4. (Original) The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

5. (Previously Presented) The method of Claim 1, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and setting the first error flag comprises setting the respective error flag associated with each defective column of RAM cells.

6. (Original) The method of Claim 5, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

7. (Original) The method of Claim 5, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

8. (Original) The method of Claim 1, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

9. (Original) The method of Claim 1, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

10. (Original) The method of Claim 1, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

11. (Previously Presented) A programmable logic device (PLD), comprising:

a first read/write data access port;

a first random access memory (RAM) circuit comprising a first array of rows and columns of RAM cells and further comprising a first redundant column of the RAM cells;

a first routing circuit coupled between the first data access port and the first RAM circuit;

wherein the first routing circuit comprises a plurality of volatile memory circuits, a plurality logic circuits, and a plurality of selector circuits, each volatile memory circuit, logic circuit, and selector circuit respectively associated with one of the columns of RAM cells;

wherein each logic circuit has a first input coupled to a respective one of the volatile memory circuits, a second input coupled to an output of a logic circuit associated with an adjacent column of RAM cells, and an output coupled to a selector input of the selector circuit;

wherein each selector circuit selects for input to the associated column of RAM cells, one of a first set of bits of configuration data addressed to the column of RAM cells and a second set of bits of configuration data addressed to the adjacent column;

a built in self test (BIST) control circuit coupled to the volatile memory circuits of the first routing circuit and further coupled to the first RAM circuit;

wherein the BIST control circuit is configured to test whether each column of RAM cells is defective, and responsive to a defective column of RAM cells, store a first value in the volatile memory circuit associated with the defective column of RAM cells;

a configuration data port; and

a configuration control circuit coupled to the BIST control circuit, the configuration data port, and the first RAM circuit.

12. (Previously Presented) The PLD of Claim 11, further comprising:

a second read/write data access port;

a second RAM circuit comprising a second array of rows and columns of the RAM cells and further comprising a second redundant column of the RAM cells; and

a second routing circuit coupled between the second data access port and the second RAM circuit,

wherein the second routing circuit comprises a plurality of volatile memory circuits, a plurality logic circuits, and a plurality of selector circuits, each volatile memory circuit, logic circuit, and selector circuit respectively associated with one of the columns of RAM cells of the second RAM circuit;

wherein each logic circuit of the second routing circuit has a first input coupled to a respective one of the volatile memory circuits of the second routing circuit, a second input coupled to an output of a logic circuit associated with an adjacent column of RAM cells of the second RAM circuit, and an output coupled to a selector input of the selector circuit of the second routing circuit;

wherein each selector circuit of the second routing circuit selects for input to the associated column of RAM cells of the second RAM circuit, one of a first set of bits of configuration data addressed to the column of RAM cells of the second RAM circuit and a second set of bits of configuration data addressed to the adjacent column of the second RAM circuit;

wherein:

the BIST control circuit is further coupled to the volatile memory circuits of the second routing circuit and to the second RAM circuit;

wherein the BIST control circuit is configured to test whether each column of RAM cells of the second RAM circuit is defective, and responsive to a defective column of RAM cells in the second RAM circuit, store a first value in the volatile memory circuit associated with the defective column of RAM cells; and

the configuration control circuit is further coupled to the second RAM circuit.

13. (Original) The PLD of Claim 11, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the first array.

14. (Original) The PLD of Claim 11, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the first array.

15. (Currently Amended) A programmable logic device (PLD), comprising:

a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

means for initiating a configuration sequence for the PLD;

means for initiating a built in self test (BIST) procedure on the first array;

means for setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array;

wherein a respective error flag is associated with each column of RAM cells in the first array;

first means for loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells; and

wherein the first means for loading comprises means for generating for each column of RAM cells a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells, and means for selecting for input to [[the]] each column of RAM cells in response to the respective selection signal, one of a first set of bits of configuration data addressed to the column of RAM cells and a second set of bits of configuration data addressed to the adjacent column.

16. (Previously Presented) The PLD of Claim 15, further comprising:

a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells;

means for initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array;

means for setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array; and

wherein a respective error flag is associated with each column of RAM cells in the second array;

second means for loading second PLD configuration data for the PLD into the second RAM circuit, wherein when the second error flag is set the second PLD configuration data bypasses the second defective column of the RAM cells and a second portion of the second PLD configuration data is loaded into the second redundant column of the RAM cells; and

wherein the second means for loading comprises means generating for each column of RAM cells in the second array a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells in the second array, and means for selecting for input to the column of RAM cells, one of a first set of bits of configuration data addressed to the column of RAM cells in the second array and a second set of bits of configuration data addressed to the adjacent column in the second array.

17. (Original) The PLD of Claim 15, wherein the means for initiating a configuration sequence for the PLD comprises means for detecting a powering up of the PLD.

18. (Original) The PLD of Claim 15, wherein the PLD is a field programmable gate array (FPGA).

19. (Previously Presented) The PLD of Claim 15, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and the means for setting the first error flag comprises means for setting the respective error flag associated with each defective column of RAM cells.

20. (Original) The PLD of Claim 19, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

21. (Original) The PLD of Claim 19, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

22. (Original) The PLD of Claim 15, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

23. (Original) The PLD of Claim 15, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

24. (Original) The PLD of Claim 15, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

25. (Currently Amended) A method of operating a programmable logic device (PLD) comprising a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells, the method comprising:

initiating operation of the PLD that has the first array configured for operation of the PLD;

initiating a built in self test (BIST) procedure on the configured first array;

resuming operation of the PLD when no errors associated with the first array are reported by the BIST procedure;

setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array;

wherein a respective error flag is associated with each column of RAM cells in the first array; [[and]]

generating for each column of RAM cells a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells; and

resuming operation of the PLD, when an error associated with the first array is reported by the BIST procedure, while using the first error flag to bypass the first defective column and to shunt read and write data from and to a first adjacent ~~the first redundant~~ column instead of the first defective column in response to the selection signal carried in from the first column.

26. (Previously Presented) The method of Claim 25, wherein the PLD comprises a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells, the method further comprising:

wherein the second array is configured for operation of the PLD;

initiating the BIST procedure on the configured second array concurrently with initiating the BIST procedure on the first array; and

setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array,

wherein a respective error flag is associated with each column of RAM cells in the second array; and

wherein resuming operation of the PLD, when an error associated with the second array is reported by the BIST procedure, comprises using the second error flag to bypass the second defective column and to shunt read and write data from and to the second redundant column instead of the second defective column.

27. (Original) The method of Claim 25, wherein the PLD is a field programmable gate array (FPGA).

28. (Previously Presented) The method of Claim 25, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and setting the first error flag comprises setting the respective error flag associated with each defective column of RAM cells.

29. (Original) The method of Claim 28, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

30. (Original) The method of Claim 28, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

31. (Original) The method of Claim 25, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

32. (Original) The method of Claim 25, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

33. (Original) The method of Claim 25, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

34. (Currently amended) A programmable logic device (PLD), comprising:

a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

means for initiating operation of the PLD that has the first array configured for operation of the PLD;

means for initiating a built in self test (BIST) procedure on the configured first array;

means for resuming operation of the PLD when no errors associated with the first array are reported by the BIST procedure;

means for setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array; and

wherein a respective error flag is associated with each column of RAM cells in the first array; and

means for resuming operation of the PLD, when an error associated with the first array is reported by the BIST procedure, while using the first error flag to bypass the first defective column and to shunt read and write data from and to a first adjacent ~~the first redundant~~ column instead of the first defective column in response to the selection signal carried in from the first column.

35. (Currently Amended) The PLD of Claim 34, further comprising:

a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells;

wherein the second array is configured for operation of the PLD;

means for initiating the BIST procedure on the configured second array concurrently with initiating the BIST procedure on the first array; and

means for setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array,

wherein a respective error flag is associated with each column of RAM cells in the second array; [[and]]

generating for each column of RAM cells a respective selection signal as a function of the error flag associated with the column and a selection signal carried in from an adjacent column of RAM cells; and

wherein the means for resuming operation comprises means for, when an error associated with the second array is reported by the BIST procedure, using the second error flag to bypass the second defective column and to shunt read and write data from and to the second redundant column instead of the second defective column.

36. (Original) The PLD of Claim 34, wherein the PLD is a field programmable gate array (FPGA).

37. (Previously Presented) The PLD of Claim 34, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and the means for setting the first error flag comprises means for setting the respective error flag associated with each defective column of RAM cells.

38. (Original) The PLD of Claim 37, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

39. (Original) The PLD of Claim 37, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

40. (Original) The PLD of Claim 34, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

41. (Original) The PLD of Claim 34, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

42. (Original) The PLD of Claim 34, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.